

Core Overview

The Avalon® Streaming (Avalon-ST) Single Clock and Avalon-ST Dual Clock FIFO cores are FIFO buffers which operate with a single clock and separate clocks for input and output ports, respectively. You can configure the cores to include Avalon Memory-Mapped (Avalon-MM) status interfaces to report the FIFO fill level.

The Avalon-ST Single Clock and Avalon-ST Dual Clock FIFO cores are SOPC Builder-ready and integrates easily into any SOPC Builder-generated systems.

This chapter contains the following sections:

- “Functional Description”
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- “Device Support” on page 13–3
- “Software Programming Model” on page 13–4

Functional Description

Figure 13–1 and Figure 13–2 show block diagrams of the Avalon-ST Single Clock and Avalon-ST Dual Clock FIFO cores.

Figure 13–1. Avalon-ST Single Clock FIFO Core

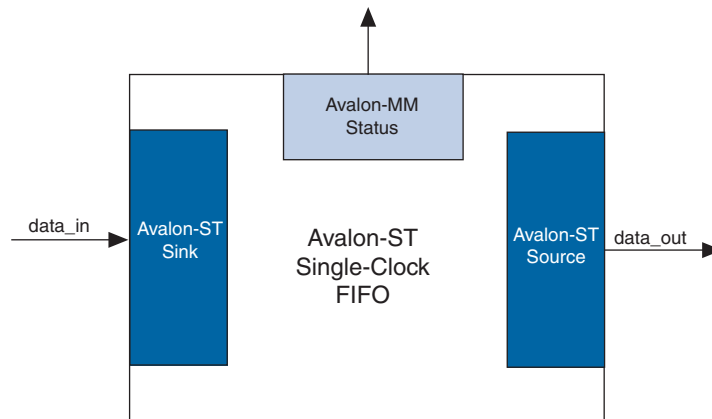
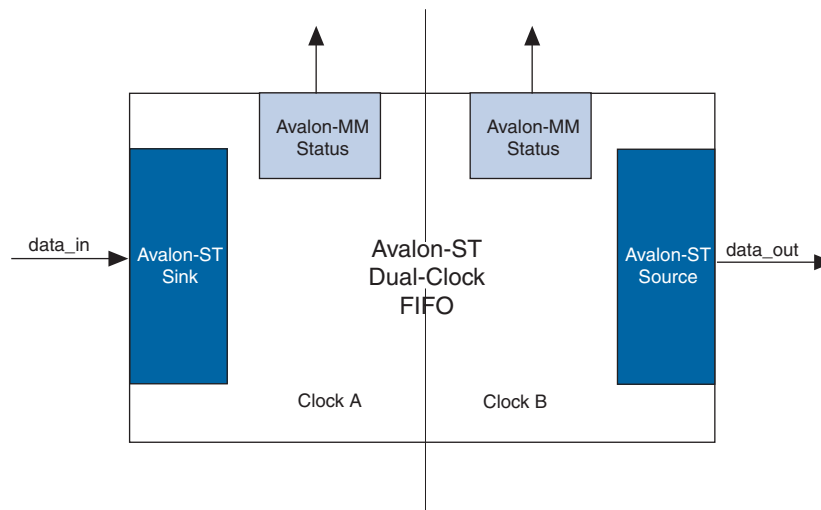



Figure 13-2. Avalon-ST Dual Clock FIFO Core

Interfaces

Table 13-1 shows the properties of the Avalon-ST interfaces.

Table 13-1. Properties of Avalon-ST Interfaces

Feature	Property
Backpressure	Ready latency = 0.
Data Width	Configurable.
Channel	Supported, up to 255 channels.
Error	Configurable.
Packet	Configurable.

 For more information about Avalon-ST interfaces, refer to the [Avalon Interface Specifications](#).

Operations

The Avalon-ST Single Clock and Avalon-ST Dual Clock FIFO cores are simple FIFO buffers with Avalon-ST input and output interfaces.

You can include an optional Avalon-MM status interface by setting the `Use_Fill_Level` parameter to 1. This interface reports the FIFO fill level. In the Dual Clock FIFO, you can implement separate status interfaces for the input and output clock domains.

Due to the latency of the clock crossing logic, the fill levels reported in the input and output clock domains may be different at any given instance. In both cases, the fill level is pessimistic for the clock domain; the fill level is reported high in the input clock domain and low in the output clock domain.

In the Avalon-ST Dual Clock FIFO, the FIFO has an output pipeline stage to improve f_{MAX} . This output stage is accounted for when calculating the output fill level, but not when calculating the input fill level. Hence, the best measure of the amount of data in the FIFO is given by the fill level in the output clock domain, while the fill level in the input clock domain represents the amount of space available in the FIFO (Available space = FIFO depth – input fill level).


Instantiating the Core in SOPC Builder

Use the MegaWizard™ interface for the Avalon-ST Single Clock and Avalon-ST Dual Clock FIFO cores in SOPC Builder to add the cores to a system.

Table 13–2 lists and describes the parameters you can configure.

Table 13–2. Configurable Parameters

Parameter	Legal Values	Description
Bits per symbol	1–32	The symbol width in bits.
Symbols per beat	1–32	The number of symbols transferred in a beat.
Error width	0–32	The width of the <code>error</code> signal.
FIFO depth	1–32	The FIFO depth. An output pipeline stage is added to the FIFO to increase performance, which increases the FIFO depth by one.
Use packets	0 or 1	Setting this parameter to 1 enables packet support on the Avalon-ST data interfaces.
Avalon-ST Single Clock FIFO Only		
Use fill level	0 or 1	Setting this parameter to 1 enables the Avalon-MM status interface.
Avalon-ST Dual Clock FIFO Only		
Use sink fill level	0 or 1	Setting this parameter to 1 enables the input clock domain Avalon-MM status interface.
Use source fill level	0 or 1	Setting this parameter to 1 enables the output clock domain Avalon-MM status interface.
Write pointer synchronizer length	2–8	The length of the write pointer synchronizer chain. Setting this parameter to a higher value leads to better metastability while increasing the latency of the core.
Read pointer synchronizer length	2–8	The length of the read pointer synchronizer chain. Setting this parameter to a higher value leads to better metastability.

 For more information on metastability in Altera devices, refer to *AN 42: Metastability in Altera Devices*. For more information on metastability analysis and synchronization register chains, refer to the *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

Device Support

The Avalon-ST Single Clock and Avalon-ST Dual Clock FIFO cores support all Altera device families.

Software Programming Model

The following sections describe the software programming model for the Avalon-ST Single Clock and Avalon-ST Dual Clock FIFO cores.

HAL System Library Support

The Altera-provided driver implements a HAL device driver that integrates into the HAL system library for Nios II systems. HAL users should access the Avalon-ST Single Clock and Avalon-ST Dual Clock FIFO cores via the familiar HAL API and the ANSI C standard library.

Register Map

The Avalon-MM status interface reports the FIFO fill level. [Table 13-3](#) shows the register map for the status interface of the cores.

Table 13-3. Register Map—Status Interface

Offset	Name	Access	Description
Base + 0	Fill Level	R	24-bit FIFO fill level. Bits 24 to 31 are unused.

Referenced Documents

This chapter references [Avalon Interface Specifications](#).

Document Revision History

[Table 13-4](#) shows the revision history for this chapter.

Table 13-4. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
November 2009 v9.1.0	No change from previous release.	—
March 2009 v9.0.0	Added description of new parameters, Write pointer synchronizer length and Read pointer synchronizer length .	—
November 2008 v8.1.0	Changed to 8-1/2 x 11 page size. No change to content.	—
May 2008 v8.0.0	Initial release.	—